REMARKS

In the final Office Action of June 14, 2004, the Examiner maintained the previous rejection of claims 1-6, 8-11, and 13-21 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,065,088 to Bronson et al. ("Bronson") and the rejection of claims 22-25 under 35 U.S.C. § 103(a) in view of Bronson. Additionally, the Examiner objected to claims 7 and 12 as being dependent on a rejected base claim, but otherwise indicated that these claims are allowable.

Applicants would like to thank the Examiner for the courtesy extended in the telephonic interview on September 15, 2004. In the interview, Applicants' representative discussed the Bronson patent as the Examiner is applying this patent to the claims, and in particular, to claim 1. Applicants' representative pointed out that Bronson does not disclose or suggest, for example, the bypass logic recited in claim 1. The Examiner agreed with the Applicants' representative on this point and agreed to reconsider the outstanding rejection in light of the interview and in light of this response, which more fully explains the differences between Bronson and the present invention.

Bronson is directed to systems and methods for interrupt command queuing and ordering. (Bronson, Title). As illustrated in Fig. 3, Bronson includes a command queue 136 for ordering EOI (end-of-interrupt) commands and a command queue 134 for ordering INR (Interrupt return) and IRR (interrupt reissue request) commands. (Bronson, Fig. 3 and col. 8, lines 9-54). Additionally, Bronson discloses a FIFO command queue 146 that orders bus memory mapped input output (MMIO) commands. (Id.)

Claim 1 recites, for example, a queue that includes a first queuing area configured to enqueue and dequeue data and a second queuing area configured to receive data from the first queuing area when the first queuing area has data available to be dequeued. Claim 1 further recites bypass logic coupled to the second queuing area, the bypass logic configured to bypass the first queuing area and to forward data to the second queuing area when the second queuing area is ready to receive data and the first queuing area is empty.

Applicants submit that Bronson fails to disclose or suggest a number of the features recited in claim 1. More specifically, Applicants submit that Bronson completely fails to disclose or suggest the bypass logic recited in claim 1. Although Bronson may disclose a number of queues, Bronson does not disclose or suggest bypass logic "configured to bypass the first queuing area and to forward data to the second queuing area when the second queuing area is ready to receive data and the first queuing area is empty" as recited in claim 1.

The queues in Bronson instead appear to be designed to prioritize different types of commands. More specifically, queue 134 of Bronson receives INR and IRR commands. Queue 136 receives EOI commands. The EOI commands are eventually dequeued from queue 136 and added to command queue 146 with incoming MMIO commands. This system is said "to enforce strict ordering of EOI commands relative to MMIO accesses." (Emphasis added) (Bronson, col. 8, lines 13-15). To summarize the sections of Bronson cited by the Examiner, Bronson prioritizes the queueing of commands, in which some types of commands are maintained in a strict queue order and other types (i.e., INR and IRR commands) are sent to a high priority queue.

Prioritizing commands, as disclosed by Bronson, does not disclose or suggest the bypass logic of claim 1. In particular, the bypass logic of claim 1 bypasses the first

queuing area when the second queuing area is ready to receive data and the first queuing area is empty. The INR and IRR commands of Bronson, in contrast, do not bypass a queue when a specific condition is met (i.e., when the second queuing area is ready to receive data and the first queuing area is empty, as recited in claim 1). Instead, they appear to be described as higher priority commands that are always transmitted to high priority output queue 150. The EOI and MMIO commands of Bronson appear to always proceed through command queue 144 and normal priority output queue 148. Thus, these commands also cannot be said to bypass a queuing area, as recited in claim 1. Accordingly, as was agreed in the interview (see Interview Summary mailed September 22, 2004), Applicants submit Bronson is significantly different than the invention recited in claim 1.

For at least these reasons, Applicants submit that Bronson does not disclose or suggest each of the features of claim 1, as required by 35 U.S.C. §102(b). Accordingly, the rejection of claim 1 should be withdrawn.

Independent claim 8 is directed to a method of masking latency in a queue. The method includes receiving incoming data items for the queue, forwarding the incoming data items to a buffer when the queue is empty and the buffer is free to receive data items, enqueuing the incoming data items in the queue when the queue contains data items or the buffer is not free to receive data items, dequeuing data items from the queue to the buffer when the buffer is free to receive data items, and transmitting the data items from the buffer as the output of the queue.

Although claim 8 does not specifically recite the word "bypass," Applicants submit that claim 8 includes features similar to those recited in claim 1 relating to the bypass logic. In particular, claim 8 includes receiving data items, forwarding the incoming data items to a buffer when the queue is empty and the buffer is free to receive data items,

and enqueuing the incoming data items in the queue when the queue contains data items or the buffer is not free to receive data items. Applicants submit that Bronson does not disclose or suggest these features of claim 8.

As discussed above, Bronson discloses high priority INR and IRR commands that are always transmitted to high priority output queue 150. Bronson also discloses EOI and MMIO commands that always proceed through command queue 144 and normal priority output queue 148. The path that these commands traverse is not conditional as to whether "the queue is empty and the buffer is free to receive data items," as is recited in claim 8.

For at least these reasons, Applicants submit that Bronson fails to disclose or suggest a number of features of claim 8, including, for example, receiving incoming data items for a queue, forwarding the incoming data items to a buffer when the queue is empty and the buffer is free to receive data items, and enqueuing the incoming data items in the queue when the queue contains data items or the buffer is not free to receive data items. Thus, the rejection of claim 8 under 35 U.S.C. § 102(b) is improper and should be withdrawn.

Independent claim 20 was rejected by the Examiner using rationale similar to that applied in rejecting claim 8. Accordingly, for reasons similar to the reasons given above with respect to claim 8, Applicants submit that the rejection of independent claim 20 is also improper under 35 U.S.C. § 102(b) and should be withdrawn.

Independent claim 14 was also rejected under § 102(b) by the Examiner based on Bronson. Claim 14 recites, among other things, "a request manager configured to receive memory requests and a plurality of parallel processors configured to receive the memory requests from the request manager." Bronson does not disclose the claimed request manager and the plurality of processors recited in this claim. System bus 100

of Bronson transmits commands to system bus control logic 100, which then forwards the commands to queues, such as queue 146. Bronson, however, completely fails to disclose or suggest a request manager and a plurality of parallel processors configured to receive the memory requests from the request manager, as recited in claim 14.

Claim 14 further recites a queue corresponding to each of the plurality of parallel processors, each of the queues configured to enqueue and dequeue memory requests of the corresponding parallel processor, and a buffer configured to receive memory requests dequeued from the queues when the queues contain memory requests and to receive memory requests directly from the input port when the queues do not contain memory requests. The Examiner appears to rely on command queue 146 and normal priority queue 148 of Bronson to allegedly disclose these features of the invention. (final Office Action, page 3). Applicants disagree with the Examiner's interpretation of Bronson. As explained previously, Bronson discloses that incoming commands are added to command queue 146, processed through command queue 146 in FIFO order, and then input to queue 148. Nothing in Bronson, however, discloses or suggests a buffer configured to receive memory requests dequeued from the queues when the queues contain memory requests and to receive memory requests directly from the input port when the queues do not contain memory requests, as recited in claim 14.

For at least these reasons, Applicants submit that the rejection of claim 14 in view of Bronson under 35 U.S.C. § 102(b) is improper and should be withdrawn.

Claims 2-6, 9-11, 13, 15-19, and 21 variously depend, either directly or indirectly, from one of independent claims 1, 8, 14, or 20. At least by virtue of their dependency on an independent claim, Applicants submit that the rejection of these dependent claims should be withdrawn.

Claims 22-25 stand rejected under 35 U.S.C. § 103(a) in view of Bronson. Applicants respectfully traverse this rejection.

Claim 22 is directed to an arbiter comprising a queue, a multiplexer, and arbitration logic. The queue is configured to enqueue data items at a first stage of a plurality of stages and dequeue the data items at a last stage of the plurality of stages of the queue. The multiplexer has a plurality of inputs connected to different stages of the queue. The multiplexer outputs selected ones of the data items read from the queue. The arbitration logic is coupled to the queue and controls the multiplexer to output the selected ones of the data items by selecting a predetermined number of data items from the queue during an arbitration cycle, the arbitration logic giving higher priority to data items in later stages of the queue.

The Examiner, in rejecting claim 22 in the final Office Action of June 14, 2004, contends that Bronson discloses a plurality of queues, but concedes that Bronson does not "teach the use of a multiplexer connected to multiple stages of a queue, outputting selected data items, and coupled to and controlled by the I/O bus control logic 152." (final Office Action, paragraph spanning pages 5 and 6). The Examiner, however, contends that this would have been an obvious modification "since multiplexers are shown to be used in the selection of signals (Figure 3, reference #144) and such a component would be useful in selecting signals from either bus 149 or bus 151 (Figure 3)." (final Office Action, page 6).

Applicants submit that the Examiner has not made a proper *prima facie* case of obviousness under § 103. Although Bronson does disclose a multiplexer 144, multiplexer 144 is not configured like the multiplexer recited in claim 22. In stark contrast, multiplexer 144 is explicitly shown as connecting only to the input of command queue 146. Bronson is completely devoid of any disclosure or suggestion to modify the

multiplexer of Bronson as suggested by the Examiner. The fact that a multiplexer can be used to "select signals" in no way discloses or suggests the multiplexer of claim 22, which "has a plurality of inputs connected to different stages of the queue." Applicants submit that the Examiner, in making the rejection of claim 22, is impermissibly using hindsight gleaned from Applicants' specification.

For at least these reasons, Applicants submit that the rejection of claim 22 under § 103 is improper and should be withdrawn. The rejection of claims 23-25, at least by virtue of their dependency on claim 22, is therefore improper and should also be withdrawn.

In view of the foregoing remarks, Applicants respectfully request the Examiner's reconsideration of this application, and the timely allowance of the pending claims.

To the extent necessary, a petition for an extension of time under 37 CFR 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

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